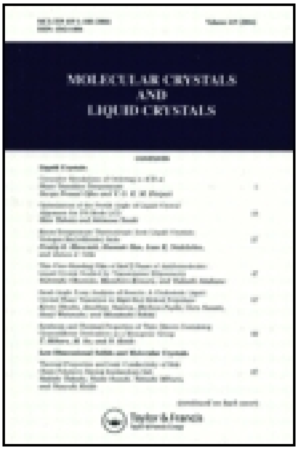

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Simulation of Fractal Immittance by Ladder Circuits

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Fractal immittance FD, expressed by an admittance ω^a with an optional value of a within the range $0 < a < 1$, is simulated by ladder circuits with finite numbers of resistors and capacitors starting from the optimized circuit based on the distributed-relaxation-time (DRT) model. Thus designed DRT-equivalent ladder with $a = 1/2$, e.g., is found to be far more effective than the conventional ladder composed of identical rungs: for the bandwidth of 5 decades with a phase-angle error of $\pm 2°$, e.g., the conventional ladder involves 6.426×10^3 identical rungs, while 11 rungs are sufficient for the DRT-equivalent circuit.

Keywords: non-integer-rank differential/integral, fractal immittance, fractance, ladder circuits

INTRODUCTION

The fractal immittance (FD) is a novel category of circuit elements, which acts as a non-integer-rank differential/integral (NIDI) operator to exhibit a unique memory effect in electric circuits.[1]–[6] The prototype of FD is the power-law conductivity (PLC), $\sigma(\omega) \propto \omega^a$ $(0 < a < 1)$. Although many materials are known to show PLC, the values of exponent are confined to $a \simeq 0.8$.[5] In this respect, several circuits have been proposed to simulate NIDI operators by the conventional elements, resistance R, capacitance C and inductance L.[2]–[6]

We have been examining the possibility of simulating FD with optional values of exponent a by Thomson cables and the related ladder circuits, which have been so far utilized as the hardware simulation of the half-integer-rank (HIDI) operators with $a=1/2$ using R and C.[2]

The ladder circuits have been designed starting from the optimized circuits based on the distributed-relaxation-time (DRT) models[6] using the continued fraction expansion. As the HIDI operators, the con-

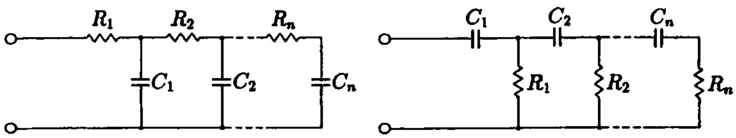

FIGURE 1. Ladder circuits with finite rungs.

ventional ladder circuits composed of identical RC rungs are found to be much less effective than thus designed DRT-equivalent ladders. Some of the results will be shown in the present paper.

OPTIMIZATION BASED ON THE DRT MODEL

The FD admittance, $Y(\omega)\propto\omega^a$ $(0<a<1)$, is rewritten as,

$$Y(\omega)=\frac{Y_F(a)\sin a\pi}{\pi}\int_{-\infty}^{+\infty}\frac{i\omega}{\lambda+i\omega}\lambda^a d(\ln\lambda), \quad (1)$$

according to the DRT model, where ω is the angular frequency, $Y_F(a)$ is a real, positive coefficient to give the magnitude, and λ refers to the relaxation rate. If Eq. (1) is approximated by a finite sum, we obtain,

$$Y_n(\omega)=\frac{Y_{Fn}(a)\sin a\pi}{\pi}\sum_{k=1}^{n}\frac{i\omega}{\lambda_k+i\omega}\lambda_k^a\Delta(\ln\lambda), \quad (2)$$

where $\Delta(\ln\lambda)=\ln\lambda_{k+1}-\ln\lambda_k$, $R_k=\pi/\{Y_{Fn}(a)\sin(a\pi)\lambda_k^a\Delta(\ln\lambda)\}$ and $C_k=1/(\lambda_k R_k)$.[3],[6] The equivalent circuit for Eq. (2) is the R_k-C_k series branches, n in number, connected in parallel one after another.

In the previous paper,[6] we have calculated the optimum pole interval $\Delta(\log\lambda)_{op}$ and the optimum bandwidth B_{op} for each n-value as

TABLE 1. Minimum numbers of R-C pairs n_{min} satisfying $a=0.5$ and $B_{op}\geq 5$ for the DRT model (left), and for the homogeneous ladder with identical rungs (right). In each DRT case, $\Delta(\log\lambda)_{op}$ is also shown.

DRT model			
ε	n_{min}	$\Delta(\log\lambda)_{op}$	B_{op}
2°	11	0.954	5.80
1°	15	0.879	5.53
1/2°	18	0.754	5.46
1/4°	23	0.680	5.65
1/8°	26	0.584	5.35

Homogeneous ladder		
ε	n_{min}	B_{op}
2°	6.426×10^3	5.00
1°	2.149×10^4	5.00
1/2°	4.776×10^4	5.00
1/4°	1.021×10^5	5.00
1/8°	2.132×10^5	5.00

TABLE 2. R_k and C_k of FD circuits synthesized using the n_{min}- and $\Delta(\log\lambda)_{op}$-values for a=0.5 and ε=2° given in Table 1. Each circuit satisfies $B \geq 5$ centered at $f_c = \omega_c/(2\pi)$ = 10^3Hz and $|Y_n(\omega_c)|$=1mS.

	DRT model		Ladder-1		Ladder-2	
k	R_k (Ω)	C_k (F)	R_k (Ω)	C_k (F)	R_k (Ω)	C_k (F)
1	3.54×10^5	2.65×10^{-5}	4.01	9.74×10^{-10}	1.63×10^5	3.97×10^{-5}
2	1.18×10^5	8.82×10^{-6}	1.01×10	2.58×10^{-9}	6.16×10^4	1.58×10^{-5}
3	3.94×10^4	2.94×10^{-6}	2.89×10	7.62×10^{-9}	2.09×10^4	5.50×10^{-6}
4	1.31×10^4	9.81×10^{-7}	8.63×10	2.28×10^{-8}	6.98×10^3	1.84×10^{-6}
5	4.38×10^3	3.27×10^{-7}	2.59×10^2	6.84×10^{-8}	2.33×10^3	6.15×10^{-7}
6	1.46×10^3	1.09×10^{-7}	7.77×10^2	2.05×10^{-7}	7.78×10^2	2.05×10^{-7}
7	4.87×10^2	3.64×10^{-8}	2.34×10^3	6.09×10^{-7}	2.61×10^2	6.80×10^{-8}
8	1.62×10^2	1.21×10^{-8}	7.12×10^3	1.79×10^{-6}	8.88×10	2.24×10^{-8}
9	5.41×10	4.04×10^{-9}	2.22×10^4	5.06×10^{-6}	3.15×10	7.16×10^{-9}
10	1.80×10	1.35×10^{-9}	7.57×10^4	1.25×10^{-5}	1.27×10	2.10×10^{-9}
11	6.02	4.49×10^{-10}	3.55×10^5	1.94×10^{-5}	8.20	4.48×10^{-10}

such that gives the largest single-domain band which fulfils a criterion with respect to the phase angle $|\mathrm{Im}Y_n(\omega)/\mathrm{Re}Y_n(\omega) - a\pi/2| \leq \varepsilon$ for a given value of deviation ε.

Table 1 shows examples of n_{min} and $\Delta(\log\lambda)_{op}$ calculated for a= 0.5 and $B_{op} \geq 5$. For ε = 2°—1/8°, n_{min} does not exceed a few tens, while $\Delta(\log\lambda)_{op}$ remains larger than half a decade.

CONTINUED FRACTION EXPANSION

Figure 1 shows two different types of ladder circuits, Ladder-1 and Ladder-2, each composed of resistors and capacitors. As is well known, the admittance is expressed using the continued-fraction expansion as,

$$Y_n(\omega) = \cfrac{1}{\alpha_1 + \cfrac{1}{\beta_1 + \cfrac{1}{\alpha_2 + \cfrac{1}{\beta_2 + \cfrac{1}{\alpha_3 + \cfrac{1}{\beta_3 + \ddots}}}}}}, \tag{3}$$

where $\alpha_k = R_k$ and $\beta_k = i\omega C_k$ for Ladder-1, and $\alpha_k = 1/(i\omega C_k)$ and $\beta = 1/R_k$ for Ladder-2. As is well known, $Y_n(\omega) \rightarrow (i\omega C/R)^{0.5}$ as $n \rightarrow \infty$ for a homogeneous ladder, i.e., with $R_k = R$ and $C_k = C$ for

$k=1,2,\cdots,n$. n_{min} for each ladder case is however by decades larger than that for the corresponding DRT case as seen in Table 1.

OPTIMIZATION OF LADDER CIRCUITS

The n_{min}-value for a ladder circuit is drastically decreased down to that for the optimized DRT circuit if we assign the appropriate values of R_k and C_k for each rung starting from Eq. (2) by employing the following procedure:
(1) Substitute the n_{min}- and $\Delta(\log\lambda)_{op}$-values for Eq. (2), and reduce it to a common denominator, i.e.,

$$Y_n(\omega)=P_n(\omega)/Q_n(\omega),\ \text{or},\ Y_n(1/\omega)=P'_{n-1}(1/\omega)/Q'_n(1/\omega), \quad (4)$$

where $P_k(x)$, $Q_k(x)$, $P'_k(x)$ and $Q'_k(x)$ are k'th-rank polynomials of x.
(2) Expand $P_n(\omega)/Q_n(\omega)$ or $P'_{n-1}(\omega)/Q'_n(\omega)$ by dividing the denominator successively by the numerator in the form of continued fraction, e.g.,

$$Y_n(\omega)=\frac{P_n(\omega)}{Q_n(\omega)}=\frac{1}{R_1+\dfrac{Q_{n-1}(\omega)}{P_n(\omega)}}=\frac{1}{R_1+\dfrac{1}{i\omega C_1+\dfrac{P_{n-1}(\omega)}{Q_{n-1}(\omega)}}}=\cdots, \quad (5)$$

for the Ladder-1 case. The values of R_k and C_k for the DRT-equivalent Ladder-2 can be determined in a similar manner.

Table 2 exemplifies the results of the numerical calculations starting from an optimized DRT circuit. The values of elements, R_k or C_k, in both optimized Ladder-1 and Ladder-2 circuits are found to reflect to some extent the fractal distribution of the original DRT circuits (i.e., a non-integer power λ^a as the weight function, see, Eq. (1)) : each set of elements roughly forms a geometric progression, showing a self-similarity, which is often referred to as one of the features of fractals. The study in this respect is now in progress and the results will be reported elsewhere.

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